AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at line 4 of page 5, as follows:

With the exception of the AND gate 16, the circuitry described thus far is conventional, and the normal operation thereof is illustrated in FIG. 2 by the ESTB, I_C and GD signals. For example, referring to FIG. 2, when the ESTB signal 40 transitions from a low to a high state, and assuming for now that the second input, OD, of the AND gate 16 is set at a high state, the gate drive circuit 18 is responsive to the resulting transition of the ESTC signal from a low to a high level to supply a high-level gate drive signal, GD, to the gate 20 of IGBT 22. IGBT 22 is, in turn, responsive to the high-level gate drive signal, GD, to begin conducting the coil current, I_C, therethrough. Because the primary coil 26 is an inductive load, the coil current I_C will rise linearly with a constant gate voltage, GD, applied to the gate 20 of IGBT 22, and the voltage across the resistor R_S will likewise rise linearly with I_C. When the voltage across R_S reaches the reference voltage, V_R, the output of the error amplifier 30 changes linearly, and the gate drive circuit 18 is responsive to this error amplifier output at the current limit input, CL, to correspondingly linearly decrease the gate drive voltage, GD, to a level at which the coil current, I_C, is limited to a constant level.